ABSTRACT

On the surface of a semiconductor material of a first conductivity type 101a, a lateral MOS transistor 100 is described surrounded by a well 171 of the opposite conductivity type and, nested within the well, an electrical isolation region 102. The semiconductor region 101a embedding this transistor has a resistivity higher than the remainder of the semiconductor material 101 and further contains a buried layer 160 of the opposite conductivity type. This layer 160 extends laterally to the wells 171, thereby electrically isolating the near-surface portion of the semiconductor region from the remainder of the semiconductor material, and enabling the MOS transistor to operate as an electrically isolated high-voltage I/O transistor for circuit noise reduction, while having low drain junction capacitance.

In the first embodiment of the invention (FIG. 1), the buried layer 171 extends vertically deeper from the surface than the electrical isolation region 102, thereby enabling a separate contact 106 to the electrically isolated near-surface portion 101a of the semiconductor region.